IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. Remarks

Information Disclosure Statement Submitted With the Filed Application.

The Examiner has not considered the information disclosure state (IDS) filed with the present application (hereinafter "IDS dated 9/8/2003").

Applicant believes the IDS dated 9/8/2003 is proper and should be considered.

Requirements for an IDS are dictated by 37 C.F.R. § 1.98:

§ 1.98 Content of information disclosure statement.

(a)(3)

(i) A concise explanation of the relevance, as it is presently understood by the individual designated in § 1.56(c) most knowledgeable about the content of the information, of each patent, publication, or other information listed that is not in the English language. ***The concise explanation may be either separate from applicant's specification or incorporated therein***.

(ii) ***A copy of the translation if*** a written English-language translation of a non-English-language document, or portion thereof, is within the possession, custody, or control of, or is readily available to any individual designated in § 1.56(c).

The above clearly indicates that a translation must be submitted only if one is in possession or readily available. Applicants would have submitted a translation if this was the case. However, this was not the case. Therefore, the Examiner's failure to accept the IDS for lack of a translation is believed to be in error.

As also emphasized above, 37 C.F.R. § 1.98 does require a concise explanation for references not in the English language. However, such a concise explanation is set forth in Applicant's Specification at Page 1, Line 13 to Page 3, Line 22.

Therefore, Applicant respectfully requests that the IDS dated 9/8/2003 be deemed as compliant with all applicable rules, and properly considered by the Examiner.

Request for Reconsideration to Establish Right of Petition.

Applicant also requests that the above be considered a formal request to reconsider the non-entry of the IDS dated 9/8/2005, to thereby establish right of petition on this matter.

Objections to Drawings

The drawings have been objected to for failing to show the subject matter of claim 9. This objection is respectfully traversed. FIG. 1 in conjunction with FIG. 2 of Applicant's Specification shows one example of the subject matter of claim 9:

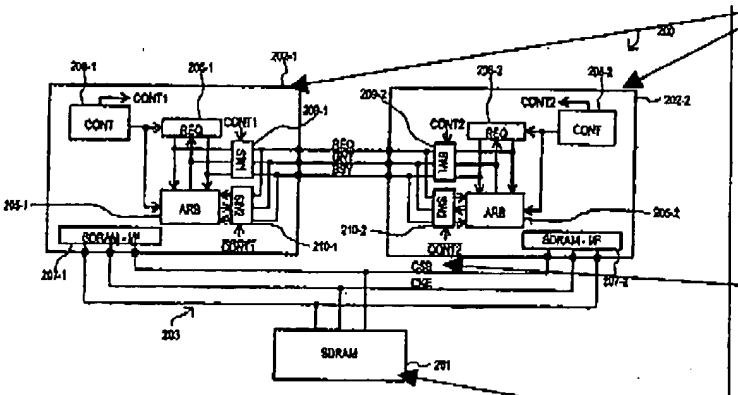

FIG. 1

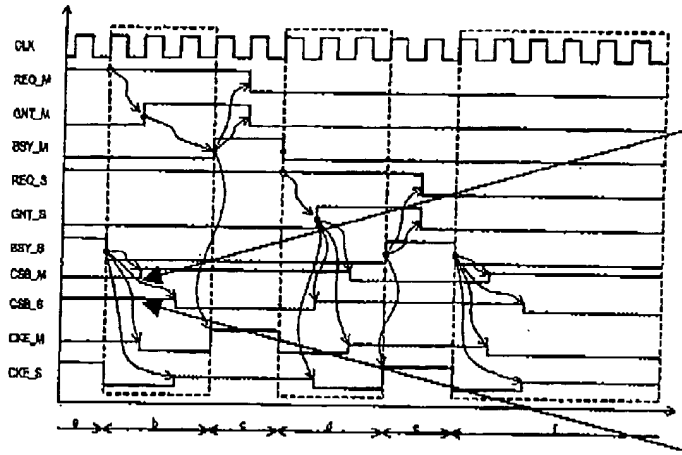

FIG. 2

A plurality of data processing circuits that share access to the semiconductor memory circuit, each having a control output coupled to

At least one control line coupled to the control input of the semiconductor memory

A semiconductor memory that is controlled by inputs to at least one control input

When one data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

When one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal

Applicant strongly stresses that the above represents but one example of how the limitations of claim are illustrated in a specific embodiment. That is, the illustrated embodiment should not be construed as limiting to the claims, as the subject matter of claim 9 could take various other forms.

Objections to the Specification

The title has been amended to address this objection.

Objections to Claims.

Claims 9 have been amended to address the claim objections. The "inputs to at least one control input" has been changed to "control signal inputs to at least one control input" for clarification.

Otherwise, the claim has been amended as suggested by the Examiner.

Rejection of Claims 1, 3, 5, 9, 10, and 14-17 Under 35 U.S.C. §103, based on Applicant's Background Art (BACKGROUND ART) in view of *Wilcox et al.* (USP 6,510,099).

The rejection of claims 1, 3, and 5 will first be addressed.

The invention of claim 1 is directed to a data processing apparatus that arbitrates sharing of a single semiconductor memory circuit among multiple data processing circuits. The data processing apparatus includes a semiconductor memory circuit and a data processing circuit supplies the semiconductor memory circuit with a clock enable signal and a chip select signal. In the data processing apparatus, before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the clock enable signal and chip select signal, a different data processing circuit starting control of the semiconductor memory circuit supplies clock enable signal and chip select signal values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[1]

[1] MPEP §2143.

The rejection admits that the BACKGROUND ART does not disclose "before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the clock enable signal and chip select signal, a different data processing circuit starting control of the semiconductor memory circuit supplies clock enable signal and chip select signal values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit", as recited in claim 1.[2]

However, the other reference relied upon by the rejection, *Wilcox et al.*, does not show such a limitation, either.

*Wilcox et al.* shows a single memory controller (106) providing control lines (324) to a plurality of memory devices in a memory system (110).[3] *Wilcox et al.* also shows that the control lines (324) include first and second chip select signal (CS_1 and CS_2) and first and second clock enable signals (CKE_1 and CKE_2). Signals CS_1 and CKE_1 go to one row of DDR SDRAM memory devices and CKE_2 go to a second row of DDR SDRAM devices.

Thus, *Wilcox* shows one controller sharing a number of memory devices. That is, there is no other device (i.e., controller, data processing circuit) that takes over control of any memory device from the memory controller (106).

For these reasons, *Wilcox et al.* is not believed to shows "a different data processing circuit starting control of a semiconductor memory circuit" "before a data processing circuit ends control of the semiconductor memory" according to the claimed signal activations, as recited in claim 1.

Further, because both reference appear silent as to such control switching operations, the cited combination of references is not believed to be suggestive of such a limitation, either.

For all of these reasons, the combination of references is not believed to show or suggest all the limitations of claim 1, and this ground for rejection are traversed.

The rejection of claims 9, 10, and 14 will now be addressed.

The data processing apparatus of amended claim 9 includes a semiconductor memory circuit that is controlled by control signal inputs to at least one control input. At least one control line is coupled to the at least one control input of the semiconductor memory circuit. A plurality

[2] See page 5, first paragraph of Office Action dated 9/21/2005.
[3] See FIG. 3 of *Wilcox et al.* showing a memory controller (106) providing control lines (324) to memory system (110).

of data processing circuits that share access to the semiconductor memory circuit, each data processing circuit having a control output coupled to the at least one control line. When one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal. Subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

To address this rejection, the arguments set forth with regard to claim 1 are incorporated herein by reference. Namely, neither reference shows or suggests "another data processing circuit" taking control over a semiconductor memory circuit from a first data processing circuit according to the control signal potentials and time periods, as recited in claim 9.

Claim14, which depends from claim 9, recites "at least one control line is directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits.

The rejection relies on the BACKGROUND ART to show the limitations of claim 14. Applicant does not believe such teachings are shown or suggested. Applicant's FIG. 4 shows two controllers 102 (i.e., data processing circuits) that provide signals via signal lines (106) and data buses (105). However, no signal lines (106) of one controller are directly connected to the outputs of multiple data processing circuits. Instead, such signals lines (106) are commonly provided to arbiter (103). Similarly, no bus lines (105) of one controller are directly connected to the outputs of multiple controllers. Instead, data buses (105) are commonly provided to bus control circuit (104).

Because the BACKGROUND ART only teaches connection to an interposing circuit, the reference is not believed to shows or suggests a direct connection, as recited in claim 14, either.

For these reasons, the combination of references is not believed to show or suggest all the limitations of claim 14, and this ground for rejection is traversed.

The rejection of claims 15–17 will now be addressed.

The invention of amended claim 15 is directed to a method of sharing a semiconductor memory circuit with a plurality of data processing circuits. The method includes, when a data processing circuit ends control of the semiconductor memory circuit, driving control outputs coupled to control lines for the semiconductor memory circuit to predetermined logic values, and

subsequently placing the control outputs in a high impedance state. The method also includes, when a data processing circuit starts control of the semiconductor memory circuit, driving control outputs coupled to control lines to the predetermined logic values prior to the control outputs of the data processing circuit that is ending control of the semiconductor memory circuit being placed in the high impedance state.

To address this rejection, the arguments set forth with regard to claim 1 are incorporated herein by reference. Namely, neither reference shows or suggests "when a different one of the plurality of data processing circuits starts control of the semiconductor memory circuit, driving control outputs prior to the control outputs of the data processing circuit that is ending control of the semiconductor memory circuit". Rather, the teachings relied upon to show the limitations of claim teach only a single controller controlling multiple memory devices.

Accordingly, because the cited combination of references is not believed to show or suggest all of the Applicant's claim limitations, this ground for rejection is traversed.

Rejection of Claims 2, 4, 6-7, 11 and 18-20 Under 35 U.S.C. §103, based on Applicant's Background Art in view of *Wilcox et al.*, and further in view of *Askinazi et al.* (USP 4,453,21).

The rejection of claims 2, 4 and 6-7 will first be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the comments set forth above for independent claim 1.

The rejection of claim 11 will now be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the comments set forth above for independent claim 9.

The rejection of claim 18-20 will now be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the comments set forth above for independent claim 15.

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Claims 1, 9 and 15 have been amended not in response to the cited art, but to address typographical errors and claim objections.

The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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